Topic 17 Hardware: Processors – Worksheet

1. Research and Present

a. Draw a diagram of a central processing unit that includes the following components: ALU, general-purpose registers, specialized registers (PC, CIR, MAR, MDR), address bus, and data bus. Show the data connections between the components **(10)**

b. If the processor above were to have an accumulator register (ACC), where would it be placed? **(1)**

An accumulator would be placed at the output of the ALU.

c. Some modern architectures, such as RISC-V do not have an accumulator register (ACC). Explain where the results of a computation are stored in such an architecture. **(1)**

The results of a computation are simply stored directly back in the general purpose registers.

(Or in the case of a load instruction, the computed address may be sent to the MAR.

d. In a reduced instruction set architecture, such as ARM or RISC-V, data is copied from memory using a load instruction.

Describe in detail the fetch-decode-execute cycle where the instruction is a load instruction. Assume the address of the data to be loaded is stored in a general-purpose register labelled GP1 and the data loaded is to be stored in a second general-purpose register labelled GP2. Include a description of the contents of the internal CPU registers change during each phase. Include the registers: PC, CIR, MAR, MDR, GP1, and GP2.

Fetch: **(6)**

PC contains address of next instruction (1) copied to MAR (1); control signals set to read

Memory responds with the instruction (1) which is loaded into the MDR (1) and then

into the CIR (1)

The PC is incremented (by 4 bytes for 32-bit ISA) to point to the next instruction. (1)

Then the decode phase may begin.

Decode: **(2)**

The control unit examines the opcode in CIR to determine what operation to perform. (1)

The load instruction has two operands (register # for address, register # for data),

so these are decoded. There are no changes to the CPU registers during decode (1).

Execute: **(3)**

The address in GP1 is copied to the MAR (1); control signals are set to read

Memory responds with data, which is stored in the MDR (1)

The contents of the MDR are then copied into GP2 (1)